A32 Channel Card Performance Specifications

Clock Jitter

The stable time base of the SIA-3000 provides the capability to perform time interval measurements over a broad time span without a significant increase in the wideband jitter noise floor. The frequency range for jitter measurements is 0.4 Hz - 3 GHz.

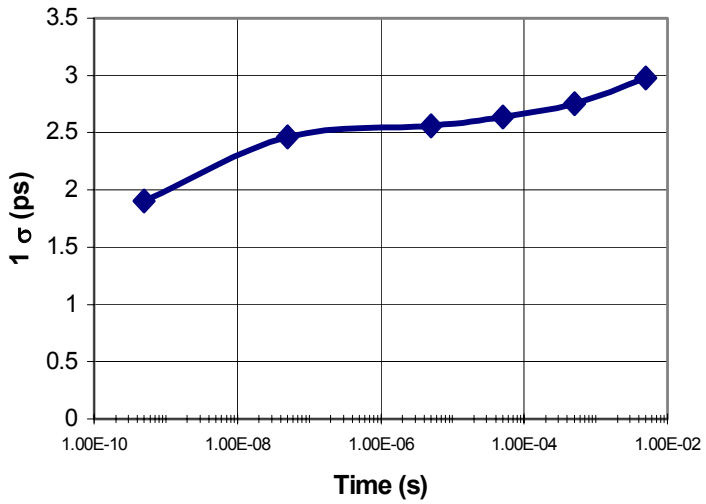
Data in Plot 1 was acquired with a 2 GHz, sine wave. Plot 1 shows the 1 σ of a histogram with 10,000 hits for time intervals ranging from 500 ps (1 period) to 5 ms (10,000,000) periods.

The guaranteed noise floor specification, is < 3 ps rms for a 1000 sample period measurement with 1.0 V_{pp}, 0.500–3 GHz differential sine wave input.

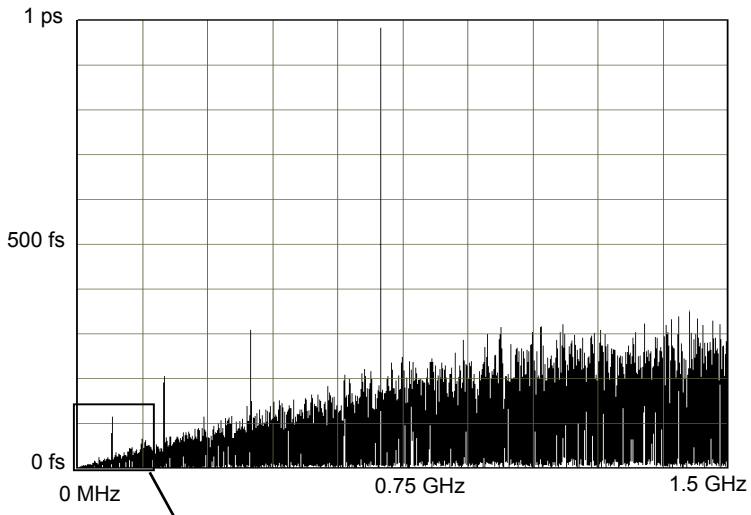
Plots 2 and 3 illustrate the typical instrument noise floor measured with the High Frequency Modulation tool in the *VISI*™ Clock analysis software module.

Plot 2 shows a spectral view of jitter measured over 1 clock period from 100 kHz to 1.5 GHz of a 3 GHz sine wave. A 700 and 80 MHz sine wave was added to the carrier. Plot 2 shows the 700 MHz spectral component with a magnitude of 1 ps. The background noise of the measurement is <300 fs over the entire frequency range.

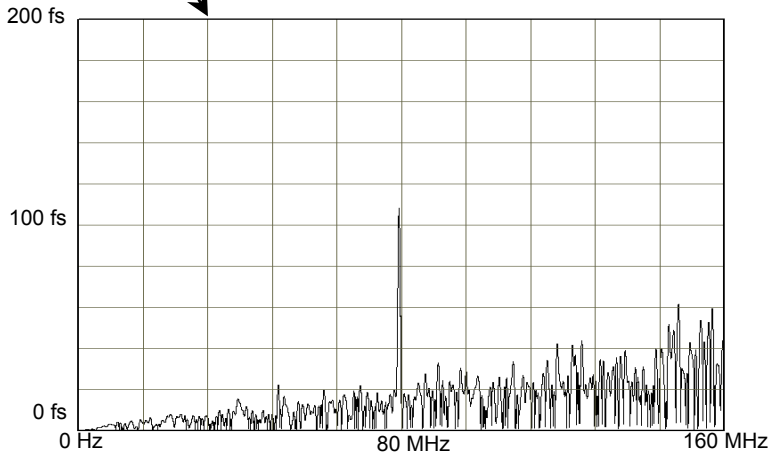
Plot 3 shows a zoomed view of plot 2 from 100 kHz to 160 MHz showing the 80 MHz spectral component. The magnitude of the 80 MHz component is 100 fs and the background noise of the measurement <60fs.



Plot 1



Plot 2

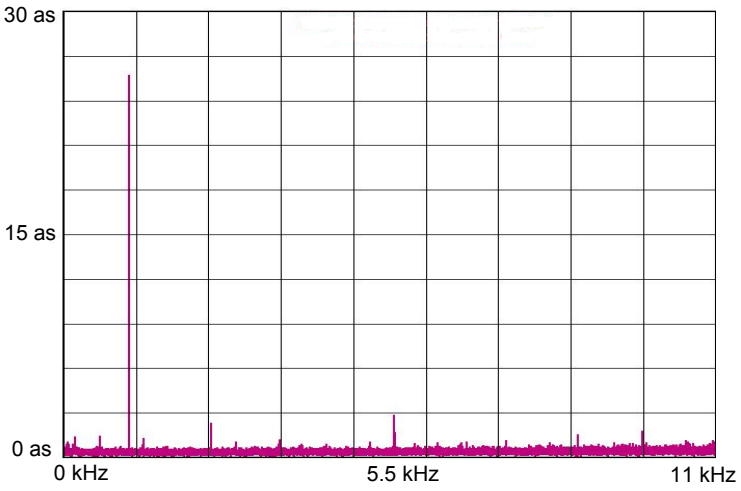


Plot 3

Plot 4 shows typical noise level using the Low Frequency Modulation tool. The Low Frequency Modulation tool provides the capability of measuring low frequency (<100 kHz) periodic components on a carrier.

Plot 4 shows spectral view of jitter over 1 clock period from 0 Hz to 10 kHz of a 2 GHz sine wave modulated with a 100 Hz peak deviation 1 kHz sine wave. The 1 kHz spectral component has a magnitude of 25 as and the background noise is <1 as.

NOTE: 1 attosecond (as) equals 10^{-18} sec.



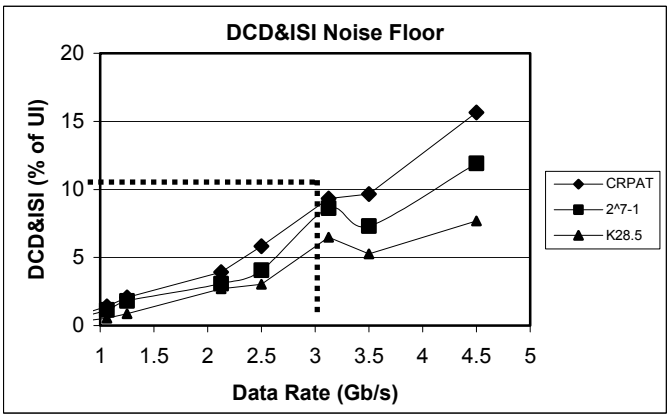
Plot 4

Data Jitter

Data Rate Range ..... up to 3.2 Gb/s

DCD&ISI Noise Floor ..... < 10% UI using CRPAT as the test pattern.

Plot 5 shows typical DCD&ISI noise floor performance at various data rates and data patterns. The dashed line represents the guaranteed DCD&ISI specification limit. The data in plot 5 includes DCD & ISI contributions from 1m of cable and from the pattern generator



Plot 5

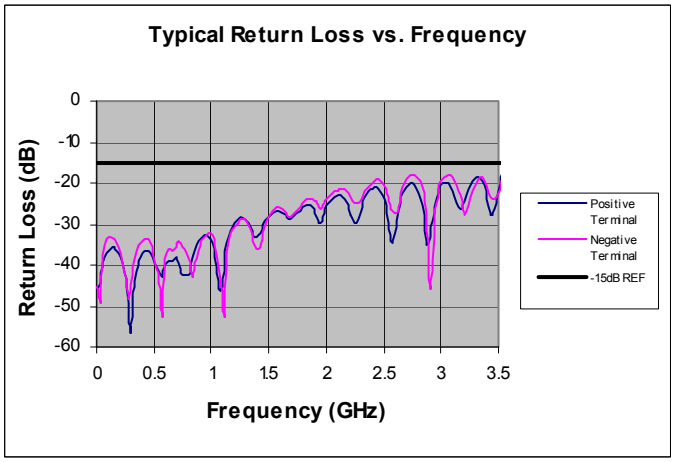
Voltage Performance

Input voltage range ..... ±1.4 V

The Input Voltage Range is defined as the minimum and maximum input voltage levels, relative to chassis ground, that the inputs can safely accept and meet performance specifications (max. differential voltage of 2.8 V).

Input Sensitivity ..... 200 mV_{pp} differential
400 mV_{pp} single-ended

Return Loss ..... With respect to 50 Ω less than –15 dB from 10 MHz to 3 GHz as shown in plot 6.



Plot 6

Note: Typical measurements provide non-warranted information about system performance or capabilities.